DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/11/08 has been entered.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. William S. Frommer on 03/24/08.

The application has been amended as follows:

As per claim 1: A method for determining a bit error rate, comprising the steps of: acquiring a data signal by an acquisition unit of a test instrument for a predetermined period of time;

storing said data signal in a memory of said test instrument;

recovering ~~a clock signal~~ a virtual clock from said stored data signal by establishing a threshold and determining pairs of adjacent samples of said stored data signal that straddle said threshold,

taking into account a hysteresis requirement to confirm that a determined pair of adjacent samples that straddle said threshold represent a threshold crossing point;

slicing said stored data signal into a plurality of data segments of a predetermined length in accordance with said recovered ~~clock signal~~ a virtual clock;

synchronizing each of said data segments to align them to a frame or predetermined pattern to determine a bit error rate thereof;

and comparing each of said data segments to said predetermined pattern on a bit by bit basis.

As per claim 2: The method of ~~processing a data signal~~ claim 1, wherein said clock recovery step further comprises the steps of:

comparing each portion of the stored data signal to said threshold level; and

estimating a time of crossing said threshold between said adjacent samples to obtain a series of observed times of threshold crossing.

As per claim 3: The method of claim 2, said clock recovery step further comprising the steps of:

comparing said series of observed times of threshold crossing to an ideal perfectly periodic sequence of expected times of threshold crossing comprising said recovered virtual ~~periodic~~ clock;

determining an error between said observed times of threshold crossing and of said series of expected times of threshold crossing comprising said recovered virtual clock based upon said comparison; and

adjusting the phase of said recovered virtual ~~periodic~~ clock in accordance with said determined error.

As per claim 10: An apparatus for determining a bit error rate, comprising:

an acquisition unit of a test instrument for acquiring a data signal for a predetermined period of time;

a memory of said test instrument for storing said data signal;

a clock recovery unit for recovering a ~~clock signal~~ virtual clock from said stored data signal by establishing a threshold and determining pairs of adjacent samples of said stored data signal that straddle said threshold, taking into account a hysteresis requirement to confirm that a determined pair of adjacent samples that straddle said threshold represent a threshold crossing point;

a processor for slicing said stored data signal into a plurality of data segments of a predetermined length in accordance with said recovered ~~clock signal~~ virtual clock;

a synchronizer for synchronizing each of said data segments to align them to a predetermined pattern; and

a bit error tester for comparing each of said data segments to said predetermined pattern on a bit by bit basis to determine a bit error rate thereof.

As per claim 12: The apparatus of claim 11, said clock recovery unit further comparing said series of observed times of threshold crossing to an ideal perfectly periodic sequence of expected times of threshold crossing comprising said recovered virtual ~~periodic~~ clock, determining an error between said observed times of threshold crossing and of said series of expected times of threshold crossing comprising said recovered virtual clock based upon said comparison, and adjusting the phase of said recovered virtual ~~periodic~~ clock in accordance with said determined error.

Drawings

3. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings are not legible. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Reasons for allowance

4. The following is an examiner's statement of reasons for allowance:

The present invention is directed to a method/apparatus for determining a bit error rate, comprising the steps of:

acquiring a data signal by an acquisition unit of a test instrument for a predetermined period of time;

storing said data signal in a memory of said test instrument;

recovering ~~a clock signal~~ a virtual clock from said stored data signal by establishing a threshold and determining pairs of adjacent samples of said stored data signal that straddle said threshold,

taking into account a hysteresis requirement to confirm that a determined pair of adjacent samples that straddle said threshold represent a threshold crossing point;

slicing said stored data signal into a plurality of data segments of a predetermined length in accordance with said recovered ~~clock signal~~ a virtual clock;

synchronizing each of said data segments to align them to a frame or predetermined pattern to determine a bit error rate thereof;

and comparing each of said data segments to said predetermined pattern on a bit by bit basis.

The prior arts of record teach a method/apparatus for determining a bit error rate, comprising the steps of: acquiring a data signal by an acquisition unit of a test instrument for a predetermined period of time; storing said data signal in a memory of said test instrument; recovering a clock signal from said stored data signal; slicing said stored data signal into a plurality of data segments of a predetermined length in accordance with said recovered clock signal; synchronizing each of said data segments to align them to a frame or predetermined pattern to determine a bit error rate thereof; and comparing each of said data segments to said predetermined pattern on a bit by bit

basis. But the prior arts of record fail to teach recovering a virtual clock from said stored data signal by establishing a threshold and determining pairs of adjacent samples of said stored data signal that straddle said threshold and taking into account a hysteresis requirement to confirm that a determined pair of adjacent samples that straddle said threshold represent a threshold crossing point.

Hence, the prior arts of record fail to anticipate or render obvious the claimed inventions of the present invention. Therefore, claims 1-18 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10: 30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis Jacques, can be reached on (571) 272-6962. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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03/24/08

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